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| ☐ | L5 | hierarchic$9 with clock with select$4 with tree | 5 |
| ☐ | L4 | (arrang$4 near5 clock) same ((based or accord$4 or depend$4) near5 (amount or number or frequency or degree) near5 (use or usage)) | 0 |
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| ☐ | L1 | hierarchic$9 with clock with select$4 | 38 |

END OF SEARCH HISTORY

L1: Entry 14 of 38 File: USPT Aug 25, 1998

DOCUMENT-IDENTIFIER: US 5799176 A
TITLE: Method and apparatus for providing clock signals to macrocells of logic devices

Brief Summary Text (16):
With this arrangement, a user may select three synchronous clock signals from a total of twelve synchronous clock signals for each logic block. The selection of the three synchronous clock signals may, and likely will, differ from logic block to logic block. Moreover, the user may program a different product term clock for each logic block. Finally, on a macrocell-by-macrocell basis, the user may select one clock signal from among the three previously selected synchronous clock signals and the single product term clock signal. Hence, substantial clocking flexibility is provided. Nevertheless, as a result of the hierarchical clocking arrangement, the total number of input clocks connected into each macrocell is only four, thus requiring only two selection bits to be transmitted to each macrocell. Accordingly, relatively minimal chip resources are required. Thus, an effective trade-off is achieved between clocking flexibility and resource requirements.

Detailed Description Text (10):
The particular choice for the values for N, M and J may depend on a variety of factors including the number of logic blocks, the number of macrocells per logic block, the number of product terms that can be processed by each macrocell, the expected applications that the CPLD may be required to perform, and the environment into which the CPLD may be required to function in, including pin-compatibility with other components. As such, the values for N, M and J may differ greatly among different implementations of CPLDs. In general, however, it is expected that N may typically be in the range from four to ten and M may typically be in the range from two to five. Also, it is expected that J will typically be one. Regardless of the particular choices for N, M and J, each CPLD configured in accordance with the invention has a generally hierarchical clock selection arrangement whereby a relatively large number of input synchronous clock signals and internally generated product term clock signals are reduced, on a logic block by logic block basis, to fewer clock signals for inputting to each macrocell. The synchronous clocks and the product term clock signals received by the macrocells are reduced, on a macrocell-by-macrocell basis, to a single clock signal for clocking each particular macrocell.

L1: Entry 10 of 38 File: USPT Aug 29, 2000

DOCUMENT-IDENTIFIER: US 6112171 A
TITLE: Methods of efficiently recording and audio signal in semiconductor memory

Brief Summary Text (12):
According to a fifth aspect of the invention, the data are reproduced at a variable clock rate, the number of hierarchical levels reproduced being selected according to the clock rate.

Detailed Description Text (44):
Referring to FIG. 12, the modified system has an address switch 45 that supplies addresses to the semiconductor memory 14 from either a write address generator 46 or a read address generator 47. Another new element is a hierarchical level selector 48 that instructs the hierarchical decoder 31 how many hierarchical levels to decode on the basis of a signal received from a clock divider 49. The clock divider 49 divides the clock signal from the clock generator 35, thereby controlling the reproducing speed. The clock divider 49 is itself controlled by a speed switch 50 comprising an up-switch for increasing the speed and a down-switch for decreasing the speed. The clock divider 49 supplies output clock signals to the hierarchical decoder 31 and the digital-to-analog converter 20. This controls the rate at which the hierarchical decoder 31 outputs digitized audio data and the digital-to-analog converter 20 converts the digitized audio data to an analog signal. The clock generator 35 also supplies clock signals to the hierarchical decoder 31 and other elements in FIG. 12, for use by computational circuits in these elements.

Detailed Description Text (48):
The hierarchical level selector 48 calculates, from the frequency division ratio of the clock divider 49, the maximum number of hierarchical levels the hierarchical decoder 31 will have time to decode at the current reproduction speed, and instructs the hierarchical decoder 31 to decode only that number of levels. Similarly, the read address generator 47 is notified of the frequency division ratio by the clock divider 49 and generates memory addresses only for data on the appropriate hierarchical levels.

CLAIMS:

5. The apparatus of claim 1, further comprising:

a digital-to-analog converter coupled to receive said digitized data from said hierarchical decoder, for converting said second digitized data to a signal;

a clock generator for generating clock signals;

a clock divider coupled to said clock generator, for dividing said clock signals according to a selectable division ratio and for supplying divided clock signals to said digital-to-analog converter;

a speed switch coupled to said clock divider, for selecting said division ratio; and

a hierarchical level selector coupled to said clock divider, for selecting a hierarchical level according to said division ratio and for notifying said hierarchical decoder thereof, thereby causing said hierarchical decoder for decode only hierarchical levels of data which are at most equal to the hierarchical level selected by said hierarchical level selector.

L1: Entry 9 of 38 File: USPT Aug 27, 2002

DOCUMENT-IDENTIFIER: US 6440780 B1
TITLE: Method of layout for LSI

CLAIMS:

1. A semiconductor integrated circuit device layout method for designing a layout of a semiconductor integrated circuit device, said semiconductor integrated circuit device including a gated clock circuit, said gated clock circuit having one gated circuit comprising a gated cell connected to a clock and a first element group connected to a clock source via said gated cell and having a second element group directly connected to said clock source, said method comprising: a net list change step of changing a net list of said gated clock circuit to a net structure wherein a cell for correcting a stage number is added between said clock source and said second element group in order to handle said second element group as another gated circuit, a gated circuit division information generation step of determining a division number of each of said respective gated circuits so that delay values become equal and of allocating a driving ability of a cell for circuit division for said each respective gated circuit by selecting the driving ability of the cell for circuit division in accordance with the total load capacitance of said each respective gated circuit based on the result of carrying out at least one of an arrangement and an appropriate wiring in accordance with a net list after a change, a gated circuit division step of forming a plurality of clusters by dividing said each respective gated circuit through clustering based on information generated in said gated circuit division information generation step and of respectively inserting cells for circuit division having the driving ability allocated in said gated circuit division information generation step in the positions wherein the load capacitance of said respective clusters becomes equal, a gated cell division step of allocating the same number of gated cells for circuit division as the number of said clusters in said each respective gated circuits, of selecting the driving ability of said gated cell for circuit division so that delay values become equal in accordance with input capacitance of said cells for circuit division and of inserting said each respective gated circuit for circuit division, and a gated cell front stage CTS step for generating a hierarchical tree between said clock source and said respective gated cell for circuit division according to a clock tree system.

L1: Entry 4 of 38 File: USPT Nov 4, 2003

DOCUMENT-IDENTIFIER: US 6643791 B1
TITLE: Clock distribution scheme in a signaling server

Detailed Description Text (44):
FIGS. 12B and 12C correspond to the other two hierarchical signal cascading schema wherein each additional level of the CDTM stage in the three-stage distribution scheme also includes appropriate multiplexers for muxing the EAS signals and selectors for selecting a particular reference clock received from the level immediately prior to it. Accordingly, the CDTM-L cards 114-L comprise a multiplexer 220 for muxing up to eight EAS signals received from the CDTM-R cards 114-R and the CDTM-C cards 114-C comprise a multiplexer 220 for muxing up to twelve EAS signals received from the CDTM-L cards 114-L. Similarly, the selectors 222 are hierarchically disposed for selecting from up to eight reference clocks from the CDTM-R cards and from up to twelve reference clocks from the CDTM-L cards.

Detailed Description Text (52):
The overall functionality of the CDTM 114 may be succinctly captured as set forth in the following: upon receiving the SFI signal from an upstream source (i.e., a higher level CDTM or the CSTG), it checks the SFI bitstream integrity and updates the outbound EAS signal accordingly; performs the alignment between the SFI and system clock if needed; automatically detects its status (Level ID) in the distribution hierarchy and sets lower Level IDs as will be described hereinbelow; receives an individual 8 KHz reference clock and Status signal for each of up to twelve ports; extracts configuration parameters from the SFI signal to control its own operation; checks for Loss of Signal (LOS) on the inputs for the 19.44 MHz clock 212 and the SFI signal 214 and, if LOS is detected, the CDTM drives the Status (i.e., EAS) and the ports high; receives EAS signals from up to twelve sources, and detects and updates hierarchical Level ID information as will be described below; checks EAS input for misalignment and, if detected, disables the appropriate shelf ID of the particular SFI output port; if Loss of Alignment (LOA), Loss of Clock (LOC), or LOS are detected, updates the CDTM's Status field; activates all alarms upon receiving the Forced Alarm bit in the SFI signal; updates CDTM fields as required, calculates BIP and transmits aligned Status; interfaces with System Alarm Assembly (SAA) card to provide control of audible as well as visual alarms; performs the reference clock selection based on the code received in the SFI and if one of the reference clock inputs is selected and that clock is lost (LOC), it reports back to the CSTG on the Status line; and generates two copies of selected 8 KHz references for the A-side and B-side CSTG pair at the highest level in the hierarchy.

L1: Entry 2 of 38 File: USPT Mar 16, 2004

DOCUMENT-IDENTIFIER: US 6707758 B2
TITLE: Semiconductor memory device including clock generation circuit

Brief Summary Text (59):
Preferably, a plurality of the data output circuits are provided, each the at least one signal recovery circuit receives the first and second operation clocks from the clock select circuit, each of the plurality of data output circuits receives the first and second operation clocks from any the at least one signal recovery circuit, and the clock select circuit, the at least one signal recovery circuit and the plurality of data output circuits are provided in a hierarchical tree structure.

CLAIMS:

3. The semiconductor memory device according to claim, wherein a plurality of said data output circuits are provided, each said at least one signal recovery circuit receives said first and second operation clocks from said clock select circuit, each of said plurality of data output circuits receives said first and second operation clocks from any said at least one signal recovery circuit, and said clock select circuit, said at least one signal recovery circuit and said plurality of data output circuits are provided in a hierarchical tree structure.